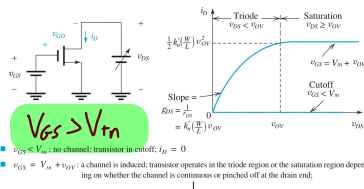


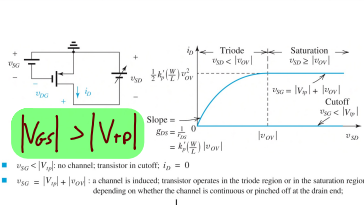
Fundamental Formulas

look for Formulas that solve for the same Variables

$V_{ov} = V_{GS} - V_{tn}$
 $I_D = \frac{1}{2} k_n \left(\frac{W}{L}\right) (V_{ov})^2 \rightarrow k_n = \mu_n C_{ox}$
 $\frac{I_x}{I_y} = \left(\frac{W/L}{W/L}\right)_x \rightarrow$ Only when Gate is shared to S/D

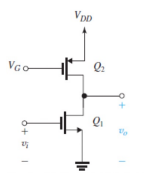


Triode Region
 Continuous channel, obtained by: $v_{DS} > |v_{GS}|$
 or equivalently: $v_{DS} > v_{GS}$
 Then: $i_D = k_n \left(\frac{W}{L}\right) \left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2 \right]$
 or equivalently: $i_D = k_n \left(\frac{W}{L}\right) \left[(v_{GS} - V_{tn})^2 - v_{DS}^2 \right]$



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 or equivalently: $i_D = k_n \left(\frac{W}{L}\right) \left[(v_{GS} - |V_{tp}|)^2 - v_{DS}^2 \right]$

CMOS



$V_G = V_{DD} - V_{GS2} = 1.8 - 0.5 - 0.2 = 1.1V$
 $(W/L)_2 = \frac{2 \cdot I_{D0}}{k_n |V_G|^2} = \frac{2 \cdot 100\mu A}{86 \mu A/V^2 \cdot 0.2^2} = 58.49$
 $(W/L)_1 = \frac{2 \cdot 100\mu A}{86 \mu A/V^2 \cdot 0.2^2} = 12.92$
 $A_{v0} = -g_{m1} (r_{o1} || r_{o2})$
 $g_{m1} = \frac{2 \cdot 100\mu A}{0.2} = 1mA/V$
 $r_{o1} || r_{o2} = \frac{A_v}{g_{m1}} = \frac{20}{1mA} = 20k\Omega = \frac{V_{DD} \cdot L}{I_D} || \frac{V_{GS} \cdot L}{I_D} = 50k\Omega || 20k\Omega = 14.3k\Omega$
 $L = \frac{20}{2 \cdot 1.8} = 0.73\mu m$

The circuit in Fig. A3 is fabricated in the 0.18- μm CMOS process whose parameters are specified in Table K.1 (Table 11. The supply voltage $V_{DD} = 1.8V$. Design the circuit to obtain a voltage gain $A_v = -20V/V$. Use devices of equal length L operating at a drain current $I_D = 100\mu A$ and $|V_{GS}| = 0.2V$. Determine the required values of V_G , L , $(W/L)_1$, and $(W/L)_2$.

Small-Signal Parameters

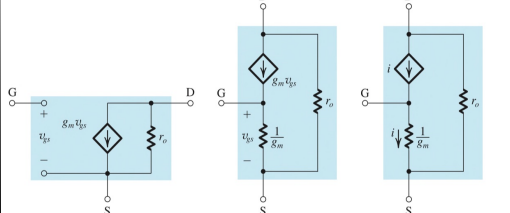
NMOS transistors

Transconductance:
 $g_m = \mu_n C_{ox} \frac{W}{L} V_{ov} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{ov}}$
Output resistance:
 $r_o = V_A / I_D = 1/k_n' \rightarrow g_{ds} = \frac{I_D}{V_{ov}}$

PMOS transistors

Same formulas as for NMOS except using $|V_{GS}|$, $|V_{GS}|$, $|I_D|$ and replacing μ_n with μ_p .

Small-Signal, Equivalent-Circuit Models



Hybrid- π model

Case	R_{i1}	R_{o2}	R_{o1}	A_{v1}	A_{v2}	A_v
1	∞	∞	r_o	$-g_m r_o$	$g_m r_o$	$-(g_m r_o)^2$
2	$(g_m r_o) r_o$	r_o	$r_o/2$	$-\frac{1}{2}(g_m r_o)$	$g_m r_o$	$-\frac{1}{2}(g_m r_o)^2$
3	r_o	$\frac{2}{g_m}$	$\frac{2}{g_m}$	-2	$\frac{1}{2}(g_m r_o)$	$-(g_m r_o)$
4	$0.2r_o$	$\frac{1.2}{g_m}$	$\frac{1.2}{g_m}$	-1.2	$0.17(g_m r_o)$	$-0.21(g_m r_o)$

Cascade Amps

T models

Other Formulas

$EI = \frac{V_{DS}}{L}$
 $\mu =$ mobility of holes/e⁻

Amp-Summary Table

Amplifier type	Characteristics				
	R_{in}	A_{v0}	R_{o1}	A_v	G_{fs}
Common source (Fig. 7.36)	∞	$-g_m R_D$	R_D	$-g_m (R_D R_L)$	$-g_m (R_D R_L)$
Common source with R_f (Fig. 7.38)	∞	$-\frac{g_m R_D}{1 + g_m R_f}$	R_D	$-\frac{g_m (R_D R_L)}{1 + g_m R_f}$	$-\frac{g_m (R_D R_L)}{1 + g_m R_f}$
Common gate (Fig. 7.40)	$\frac{1}{g_m}$	$g_m R_D$	R_D	$g_m (R_D R_L)$	$\frac{R_D R_L}{R_{in} + 1/g_m}$
Source follower (Fig. 7.43)	∞	1	$\frac{1}{g_m}$	$\frac{R_D}{R_D + 1/g_m}$	$\frac{R_D}{R_D + 1/g_m}$

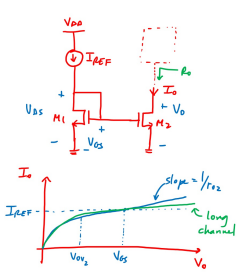
General: $\frac{V_i}{i_i} \quad \frac{V_o}{i_o} \quad \frac{V_o}{V_i} \quad \frac{V_o}{V_{S1}}$

More Formulas

$V_A = \frac{1}{\lambda} / I_D = \frac{1}{\lambda I_D}$
 $\chi \Rightarrow$ used for Body Effect
 $\rightarrow g_{mb} = \chi g_m$
 $\rightarrow A_v = \frac{1}{1 + \chi}$
 $\gamma \approx 0.4 \sqrt{V}$

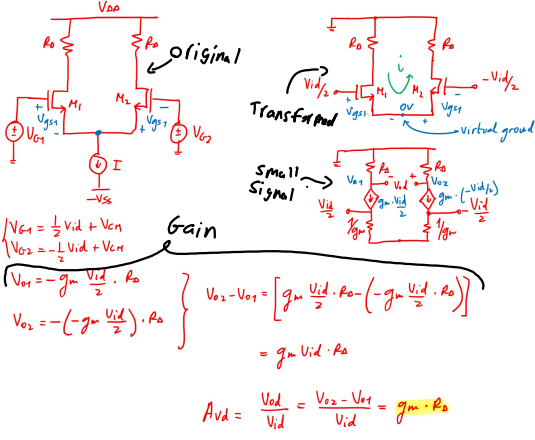
Current Mirrors

CURRENT MIRROR WITH CURRENT SOURCE I_{REF}



M_2 in SAT \rightarrow high r_o
 M_1 in SAT \rightarrow diode connected
 For M_2 to be in SAT
 $V_o \geq V_{GS} - V_t = V_{ov2} = \sqrt{\frac{2I_{D0}}{k_n (W/L)_2}}$
 output resistance $R_o = r_{o2}$
 $I_o = I_{REF}$ for $V_o = V_{oc}$
 $I_{REF} = \frac{1}{2} k_n \left(\frac{W}{L}\right)_1 V_{ov1}^2 (1 + \lambda V_{ov1})$
 $I_o = \frac{1}{2} k_n \left(\frac{W}{L}\right)_2 V_{ov2}^2 (1 + \lambda V_{ov2})$
 $\frac{I_o}{I_{REF}} = \frac{(W/L)_2 (1 + \lambda V_{ov2})}{(W/L)_1 (1 + \lambda V_{ov1})} \lambda \approx 1/2$

Differential Amps Sample

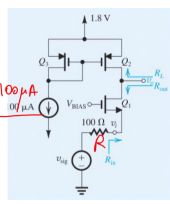


Gain
 $V_{o1} = \frac{1}{2} V_{id} + V_{en}$
 $V_{o2} = -\frac{1}{2} V_{id} + V_{en}$
 $V_{o1} = -g_m \frac{V_{id}}{2} \cdot R_o$
 $V_{o2} = -(-g_m \frac{V_{id}}{2}) \cdot R_o$
 $V_{o2} - V_{o1} = [g_m \frac{V_{id}}{2} \cdot R_o - (-g_m \frac{V_{id}}{2} \cdot R_o)] = g_m V_{id} \cdot R_o$
 $A_{vd} = \frac{V_{od}}{V_{id}} = \frac{V_{o2} - V_{o1}}{V_{id}} = g_m \cdot R_o$

EXERCISE **Amps**

$I = 20 \mu A$
 $R_S = 20 k\Omega$
 $V_{DD} = 2V$
 $K_n(W/L) = 1 mA/V^2$
 $V_T = 0.4V$
 $\lambda = 0, \gamma = 0$

- (a) $V_{id} = 0$
 $V_{CM} = V_{GS1} + V_S = V_{GS1} + I \cdot R_S$
 $V_{GS1} = V_T + V_{OV} = V_T + \sqrt{\frac{I}{K_n(W/L)}} = 0.4 + \sqrt{\frac{20 \mu A}{1 mA}} = 0.54V$
 $V_{CM} = 0.54 + 20k \cdot 20 \mu A = 0.94V$
- (b) $A_d = g_m \cdot R_o$
 $g_m = \frac{2I_D}{V_{OV}} = \frac{20 \mu A}{0.14} = 142 \mu A/V$
 $R_o = \frac{1S}{142 \mu A} = 7.04 k\Omega$
- (c) $V_{D1} = V_{D2} = V_{DD} - I_{D1} \cdot R_o = 2 - 10 \mu A \cdot 10.7 k\Omega = 0.93V$
- (d) $\frac{V_{S1}}{V_{in}} = -\frac{R_o}{\frac{1}{g_{m1}} + 2R_S} = -\frac{10k}{\frac{1}{142 \mu A} + 40k} = -2.26 V/V$ $R_o > 2R_S$
- (e) $R_{CM} = \frac{1S}{0.27} = 3.7 k\Omega$
 $CMRR = \frac{1S}{0.27} = 55.5 \rightarrow 35dB$



In the common-gate amplifier circuit of Fig. A8, Q_1 and Q_2 are matched. $K_n(W/L)_1 = K_n(W/L)_2 = 8 mA/V^2$ and all transistors have $|V_T| = 0.5V$ and $|VA| = 5V$.

The signal v_{sig} is a small sinusoidal signal with no dc component.

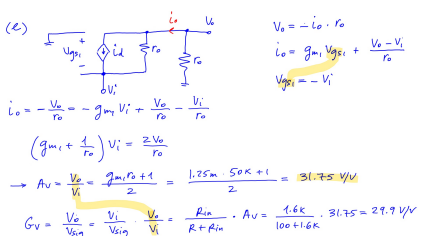
(a) Neglecting the effect of V_{cb} , find the dc drain current of Q_1 and the required value of V_{bias} .

(b) Find the values of g_{m1} and r_{o1} for all transistors.

(c) Find the values of R_{in} and R_{out} .

(d) Calculate the voltage gains v_{D1}/v_{sig} and v_{D2}/v_{sig} .

- A5.8**
 $V_{OV} = 0.16V$
 (a) $I_1 = I_2 = I_3 = 100 \mu A$
 $V_{bias} = V_{GS1} + I \cdot R = 0.5 + \sqrt{\frac{2 \cdot 100 \mu A}{8 mA/V^2}} + 100 \mu A \cdot 100 = 0.67V$
- (b) $g_{m1} = \frac{2 \cdot 100 \mu A}{0.16} = 1.25 mA/V$
 All transistors will have the same r_o (why?)
 $r_{o1,2,3} = \frac{|VA|}{I_D} = \frac{5}{100 \mu A} = 50 k\Omega$
- (c) Small-signal eq. needed to determine R_{in} & R_{out} (See Lecture 11) \times A5.5
 $R_{in} = \frac{1 + r_{o1}/r_{o1}}{g_{m1} + 1/r_{o1}} \approx \frac{2}{g_{m1}} = 1.6 k\Omega$ { Since $r_{o2} = r_{o1}$ or $1/r_{o1} \approx 0$
- $R_o = r_o + R + g_m R R = 50k + 100 + 1.25m \cdot 50k \cdot 100 = 56.4 k\Omega$



(c) $V_o = -i_o \cdot r_o$
 $i_o = g_m v_{gs1} + \frac{V_o - V_i}{r_o}$
 $V_{gs1} = -V_i$
 $i_o = -\frac{V_o}{r_o} = -g_m V_i + \frac{V_o - V_i}{r_o}$
 $(g_m + \frac{1}{r_o}) V_i = \frac{2V_o}{r_o}$
 $A_v = \frac{V_o}{V_i} = \frac{g_m r_o + 1}{2} = \frac{1.25m \cdot 50k + 1}{2} = 31.75 V/V$
 $G_v = \frac{V_o}{V_{sig}} = \frac{V_i}{V_{in}} \cdot \frac{V_o}{V_i} = \frac{R_{in}}{R + R_{in}} \cdot A_v = \frac{1.6k}{100 + 1.6k} \cdot 31.75 = 27.9 V/V$

A4.10
 Design the circuit in Fig. 10 to obtain $I = 1 \mu A$, $I_D = 0.5 mA$, $V_S = 2V$, and $V_D = 5V$. The NMOS transistor has $V_T = 0.5V$, $k_n = 4 mA/V^2$, and $\lambda = 0$.

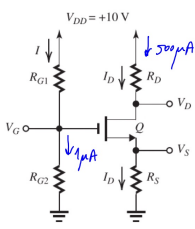


Fig. 10

$V_S = I_D \cdot R_S \rightarrow R_S = \frac{V_S}{I_D} = \frac{2}{0.5m} = 4 k\Omega$
 $V_{D0} = V_{D0} - I_D R_o \rightarrow R_o = \frac{10 - 5}{0.5m} = 10 k\Omega$
 $V_{GS} = V_T + \sqrt{\frac{2I_D}{K_n(W/L)}} = 0.5 + \sqrt{\frac{2 \cdot 0.5m}{4m}} = 1V$
 Assume SAT
 $V_{OV} = 1 - 0.5 = 0.5V < V_{DS} = 3V$ SAT ✓
 $V_{G0} = V_S + V_{GS} = 2 + 1 = 3V$
 $R_{G2} = \frac{V_{G0}}{I} = \frac{3}{1 \mu A} = 3 M\Omega$
 $R_{G1} = \frac{V_{D0} - V_{G0}}{I} = \frac{10 - 3}{1 \mu A} = 7 M\Omega$

A6.5

Design the circuit in Fig. 5 to obtain a dc voltage of 0V at each of the drains of Q_1 and Q_2 when $V_{GS1} = V_{GS2} = 0V$. Operate all transistors at $V_{OV} = 0.15V$ and assume that $V_{th} = 0.35V$ and $K_n = 400 \mu A/V^2$. Neglect channel-length modulation.

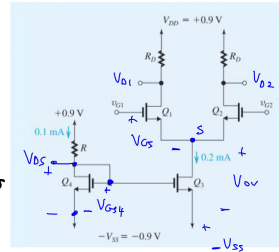


Fig. 5

Determine the values of R , R_D , and the W/L ratios of Q_1 , Q_2 , Q_3 , and Q_4 . What is the input common-mode voltage range for your design?

ICMR
 Range for which MosFets stay in Sat

A6.5 To have $V_{D1} = V_{D2} = 0V$ the voltage drop across R_D must be 0.9V

$R_D = \frac{0.9}{I_1} = \frac{2 \cdot 0.9}{0.2m} = 9 k\Omega$
 $(W/L)_{1,2} = \frac{2I_1}{K_n \cdot V_{OV}^2} = \frac{0.2m}{400 \mu A/V^2 \cdot 0.15^2} = 22.2$
 $(W/L)_3 = \frac{2I_3}{K_n V_{OV}^2} = \frac{2 \cdot 0.2m}{400 \mu A/V^2 \cdot 0.15^2} = 44.4$
 $(W/L)_4 = (W/L)_3 / 2 = 22.2$ ← M_4 carries half the current of M_3

KVL around R_D

$V_{D0} - I_4 R - V_{DS4} - (-V_{SS}) = 0$
 $V_{DS4} = V_{GS4} = V_{OV} + V_T = 0.15 + 0.35 = 0.5V$
 $R = \frac{0.9 - 0.5 - (-0.9)}{0.1m} = 13 k\Omega$

ICMR • $V_{CM, min}$ to keep M_3 in saturation

$V_{CM, min} = V_{GS1} + V_{OV} - (-V_{SS}) = V_T + 2V_{OV} - (-V_{SS}) = -0.25V$
 • $V_{CM, max}$ to keep M_1 & M_2 in saturation
 $V_{D1} - V_S > V_{CM} - V_S - V_T$
 $V_{CM, min} = V_{D1} + V_T = 0 + 0.35V = 0.35V$